Amendments to the Specification:

Please replace paragraph beginning on page 12, line 1 with the following amended paragraph:

FIG. 2 shows a processor/buffer pair relying on a common source clock. In FIG. 2, a processor 320 receives its clock from a controller 322 and data from a buffer 318. A master clock signal is provided to the controller 322. A buffer 324 accepts data generated by the processor [[310]] 320. The data is gated by a write signal from the controller 322, and the buffer [[318]] 324 provides a buffer fill level feedback signal to the controller 322 such as BUFFER_FULL, BUFFER_EMPTY, or in between, for example. Based on the buffer fill level feedback signal, the controller 322 can vary the clock signal to the processor 320 and the buffers 318 and 324 to increase or decrease the processing speed of the processor 320, thereby adjusting the read rate from the buffer 318 and the fill rate to the buffer 324.